Reg. No. : | | | | | | | | | | | | |

**Question Paper Code : 25076**

B.E. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Third Semester

Electronics and Communication Engineering

EC 8392 — DIGITAL ELECTRONICS

(Common to B.E. Medical Electronics/B.E. Computer and Communication Engineering/B.E. Mechatronics Engineering/B.E. Robotics and Automation Engineering)

(Regulations 2017)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Subtract $(1010)_2$ from $(1000)_2$ using 2's complement method. Subtract by direct method also and compare.

2. Interpret the function $Y = A + \overline{B}\,C$ in canonical POS.

3. Draw the full adder circuit.

4. What do you mean by parity checker?

5. Draw the circuit diagram of 4-bit ring counter using D'-flip flop.

6. Define shift register.

7. Draw the general model of ASM.

8. Outline critical race.

9. Interpret Read and Write operation.

10. What is programmable logic array? How it differs from ROM?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Find the MSOP representation for

$F(A,B,C,D,E) = \sum m(1,4,6,10,20,22,24,26) + \sum d(0,11,16,27)$

using K-Map. Draw the circuit of the minimal expression using only NAND gates. (8)

(ii) Implement $Y = \overline{AB} + A + \overline{(B+C)}$ using NAND gates only. (5)

Or

(b) What are the advantages of using Quine McCluskey method? Determine the Minimal sum of products for the Boolean expression

$f(A,B,C,D) = \Sigma m(1, 2, 3, 9, 12, 13, 14) + \Sigma d(0, 7, 10, 15)$

using Quine McCluskey Tabular method. (13)

12. (a) (i) With neat circuit diagram, explain the working principle of 4-bit parallel Adder/Subtractor. (8)

(ii) Illustrate the concept of basic 4-input Multiplexer. (5)

Or

(b) Design and describe the operation of 3-bit magnitude comparator. (13)

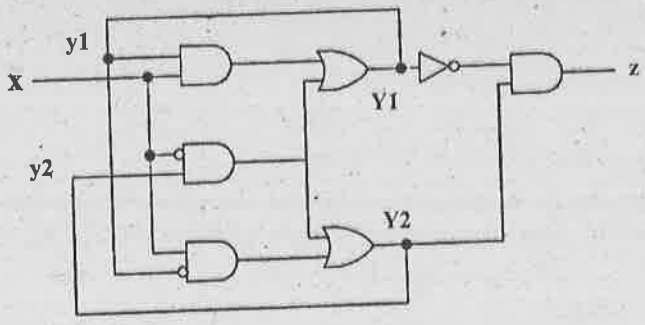
13. (a) (i) Explain the operation of JK flip-flop with neat diagram. (7)

(ii) Explain the operation of master slave flip flop and show, how the race around condition is eliminated. (6)

Or

(b) Explain the operation of synchronous MOD-6 counter. (13)

14. (a) (i) Write logical equations and construct transition table for the circuit output in terms of the circuit inputs and secondary variable. (6)




(ii) Explain Race - Free state Assignment in detail, with an example. (7)

Or

(b) (i) Draw timing diagram and explain the types of hazard in detail. (7)

(ii) Explain pulse mode sequential circuit in detail. (6)

15. (a) Differentiate static and dynamic RAM. Draw the circuits of one cell of each and explain its working. (13)

Or

(b) Illustrate the circuit operation and characteristics of TTL NAND logic gate in detail. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Design a synchronous sequence detector that produces an output 1, whenever the non overlapping sequence 1011 is detected. (15)

Or

(b) Design an even parity generator, that generates an even parity bit for every input string of 3-bits. (15)

———————